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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,433	03/12/2004	Soichi Homma	04329.3269	6546

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EXAMINER	
SANDVIK, BENJAMIN P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,433	HOMMA, SOICHI	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-20* is/are pending in the application.

4a) Of the above claim(s) *9-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Capote et al (U.S. Patent #6121689), in view of Lin (U.S. Patent #6426556).

With respect to **claim 1**, Capote teaches a semiconductor chip having a semiconductor element or an integrated circuit formed in the semiconductor chip (Fig. 15, 10), a low dielectric constant insulating film having a relative dielectric constant of about 3.5 or less formed directly on a surface of the dielectric chip (Col 10 Ln 40-41; benzocyclobutene, which is disclosed in the specification of this application to be a suitable material. It is inherent that benzocyclobutene has a dielectric constant of about 3.5 or less); a plurality of bump electrodes (Fig. 15, 14) provided on a surface of the insulating, a wiring board (Fig. 15, 20) having a plurality of connecting electrodes being electrically connected to the bump electrodes (Fig. 15, 12); and a resin molding filled in a space between the semiconductor chip and the wiring, the electrically connected bump electrodes and the connecting electrodes being arranged in the space (Fig. 15, 22), wherein the resin molding is formed a resin having a flux function and changed from liquid to solid when the bump electrodes are in a molten state (Col 4 Ln 14-24).

Capote does not teach a low dielectric constant insulating film formed on a surface of the semiconductor chip, and additionally a passivation film formed on a surface of the low dielectric constant insulating film. Lin teaches a low dielectric insulating film on a semiconductor surface (Fig. 15, 29), a passivation film formed on the insulating film (Fig. 15, 32), and that the passivation film can comprise multiple layers (Col 6 Ln 31-33). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide an additional passivation film on the film of Capote as taught by Lin in order to provide additional surface protection for the chip.

With respect to **claim 3**, Capote teaches a low dielectric constant insulating film benzocyclobutene, which is disclosed in the specification of this application to be a suitable material. It is inherent that benzocyclobutene has an adhesion strength of 15 J/m^s or less.

With respect to **claim 5**, Capote teaches that the resin has a coefficient of elasticity of greater than 20 MPa at normal temperature (Col 10 Ln 56-57).

With respect to **claim 6**, Capote teaches a resin molding comprising a first resin layer close to the semiconductor chip (Fig. 13, 37) and a second resin layer close to the wiring board (Fig. 13, 39), and the second resin layer is a resin layer which does not contain a filler (Col 9 Ln 31-32).

With respect to **claim 7**, Capote teaches a resin molding comprising a first resin layer close to the semiconductor chip (Fig. 15, 32), a second resin layer close to the wiring board (Fig. 15, 34), and a third resin layer interposed between

the first resin layer and the second resin layer (Fig. 15, 22), and the third resin layer is a resin layer which does not contain filler (Col 9 Ln 55-56, portion 39 contains no filler).

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Capote and Lin, in view of Mistry et al (U.S. Patent #6077726).

With respect to **claim 8**, Capote and Lin teach all of the limitations of claim 1, and furthermore Capote teaches that the bump electrodes of the semiconductor chip are electrically connected to a plurality of connecting electrodes formed on the semiconductor chip (Fig. 4, 24), but does not teach that a part of the connecting electrodes are coated with a passivation film comprising at least one layer formed of an organic film. Mistry teaches a passivation film comprising at least one layer formed of an organic film coating a connecting electrode (Fig. 1, 16). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Capote with a passivation layer of organic material as taught by Mistry in order to reduce stress in the package.

Response to Arguments

Applicant's arguments filed 5/15/2006 have been fully considered but they are not persuasive. In regard to the rejection of claim 1, the applicant argues that the combination of the Capote and Lin references does not teach every element of the claim. In order to clarify the rejection the examiner reiterates that the passivation layer

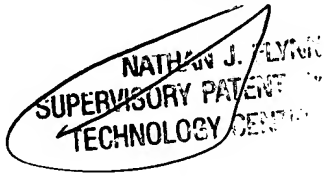
of Capote is being interpreted as the "low dielectric constant insulating film" of claim 1. The Lin reference teaches a multilayer passivation layer, and in combining this feature with the Capote reference the passivation layer of Capote is "low dielectric constant insulating film" of the claim and the additional passivation layer taught by Lin is the "passivation film" of the claim. Furthermore, the applicant argues that a passivation layer is "a layer which is not directly formed on a surface of a semiconductor chip, but on a circuit component". The examiner respectfully disagrees with this statement. While a passivation layer can surely be formed on a circuit component it is by no means the only application of a passivation layer in this art. Any surface in a semiconductor device can be passivated in order to prevent the corrosion of that surface; for example, the chip itself as taught by the Capote reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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